MOSTEK®

SINGLE-CHIP MICROCOMPUTER COMPARATIVE ANALYSIS

	MK3870	MK3875	MK3873	6805	6801	8048	8051	Z8
ROM:								
1K bytes	x		x	(1.1)		x		
2K bytes	x	x	x		x	x		x
3K bytes	x							
4K bytes	x	x					x	
RAM:								
64 bytes	x		x	x		x		
128 bytes	x	x	x		x	x		(144)
256 bytes							x	
Max Memory On-Chip	4K	4K	2K	1.1K	2K	2K	4K	2K
Parallel I/O (bits)	32	30	29	20	24	24	32	28
Serial I/O	Software	Software	Hardware USART	Software	Hardware UART	Software	Hardware UART	Hardware UART
Timer Modes								
Counter/Timer	x	x	x	x	x	x	x	x
Event Counter	x	x	x		x	x	x	x
Pulse Width	x	x	x		x			x
Software Compatible Family	Yes	Yes	Yes	No	No	Yes	No	No
Emulation:								
Piggyback EPROM	x	x	x					x
(Max Address)	4K	4K	4K					2K
On-Chip EPROM					x	x		
(Max Address)					2K	1K		
PC Board							x	

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PRELIMINARY

MOSTEK®

3870 SINGLE CHIP MICRO FAMILY

MK3870 and MK38P70

MK3870 FEATURES

- Available with 1K, 2K, 3K, or 4K bytes of mask programmable ROM memory
- 64 bytes scratchpad RAM
- Available with 64 bytes executable RAM
- 32 bits (4 ports) TTL compatible I/O
- Programmable binary timer
  Interval timer mode
  Pulse width measurement mode
  Event counter mode
- External interrupt input
- Crystal, LC, RC, or external time base options
- Low power (275 mW typ.)
- Single +5 volt supply

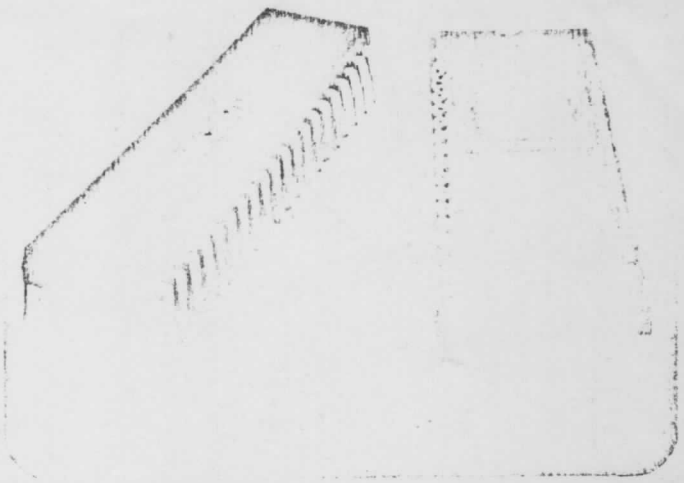
MK38P70 FEATURES

- EPROM version of MK3870
- Piggyback PROM (P-PROM)™ package
- Accepts 24 pin or 28 pin EPROM memories
- Identical pinout as MK3870
- In-Socket emulation of MK3870

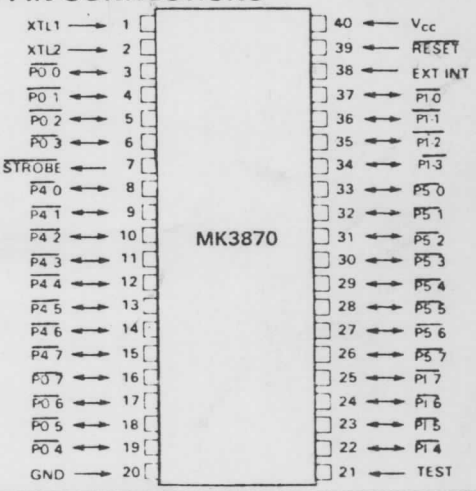
GENERAL DESCRIPTION

The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MK3870 can execute a set of more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK3870 features 1-4K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK3870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of I/O.

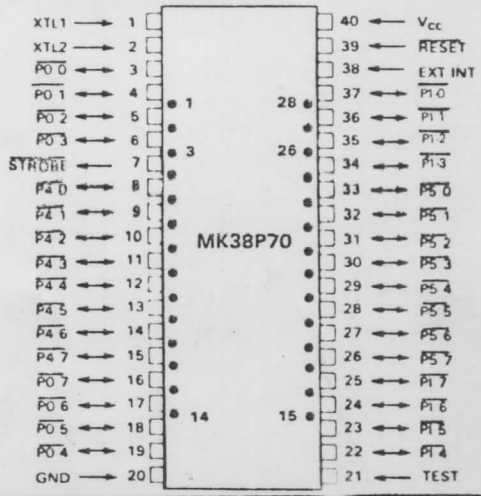
The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the



MK3870 PIN CONNECTIONS

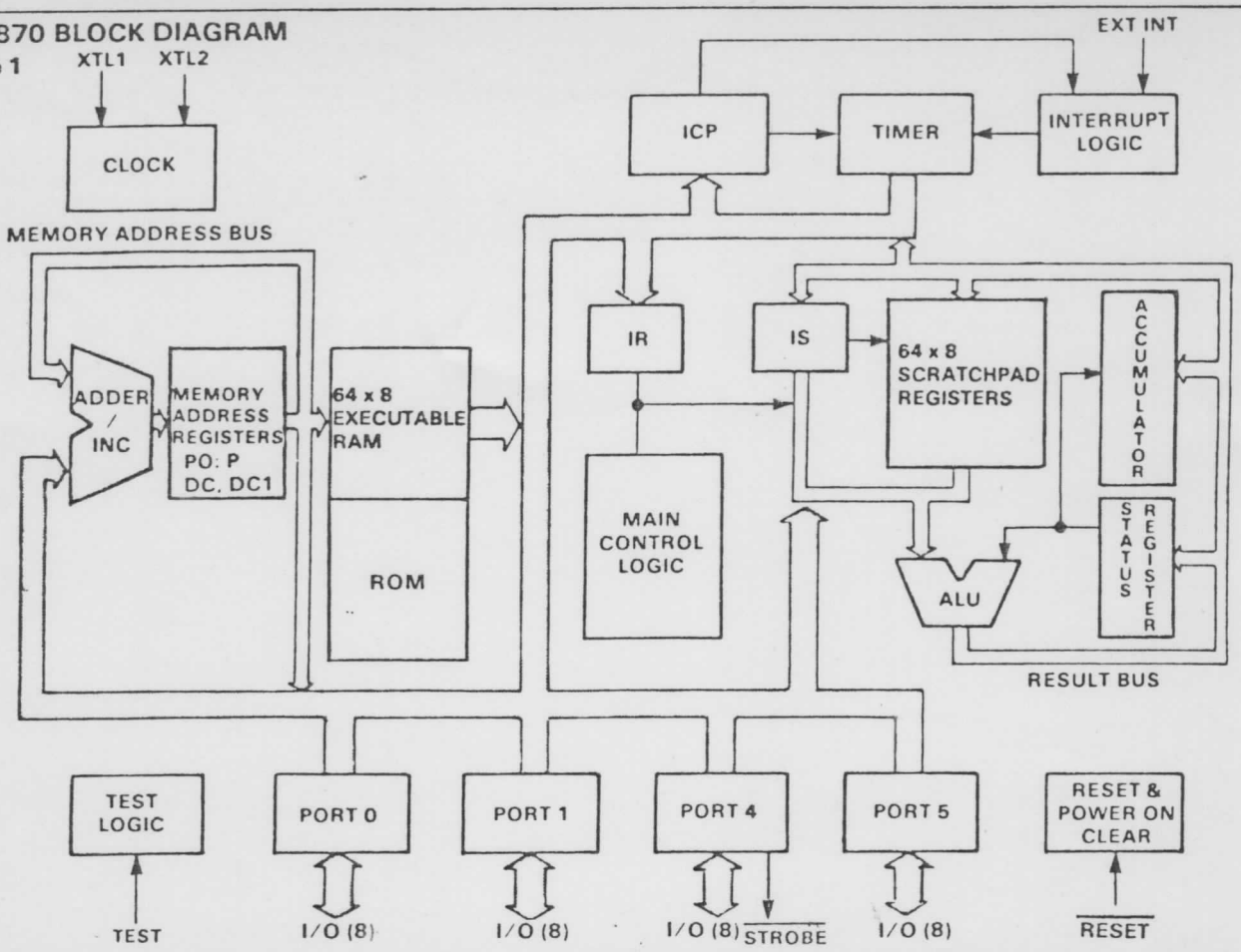


MK38P70 PIN CONNECTIONS



MK3870 BLOCK DIAGRAM

Figure 1



event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK3870 and MK38P70: Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

The MK38P70 microcomputer is the PROM based version of the MK3870. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P70 retains exactly the same pinout and architectural features as other members of the 3870 family. The MK38P70 is discussed in more detail in a later section.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$ -- $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ -- $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{\text{STROBE}}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{\text{RESET}}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$-- $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$--$\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$--$\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{\text{STROBE}}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{\text{RESET}}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.

TEST is an input, used only in testing the MK3870. For normal circuit functionality this pin may be left

unconnected, but it is recommended that TEST be grounded.

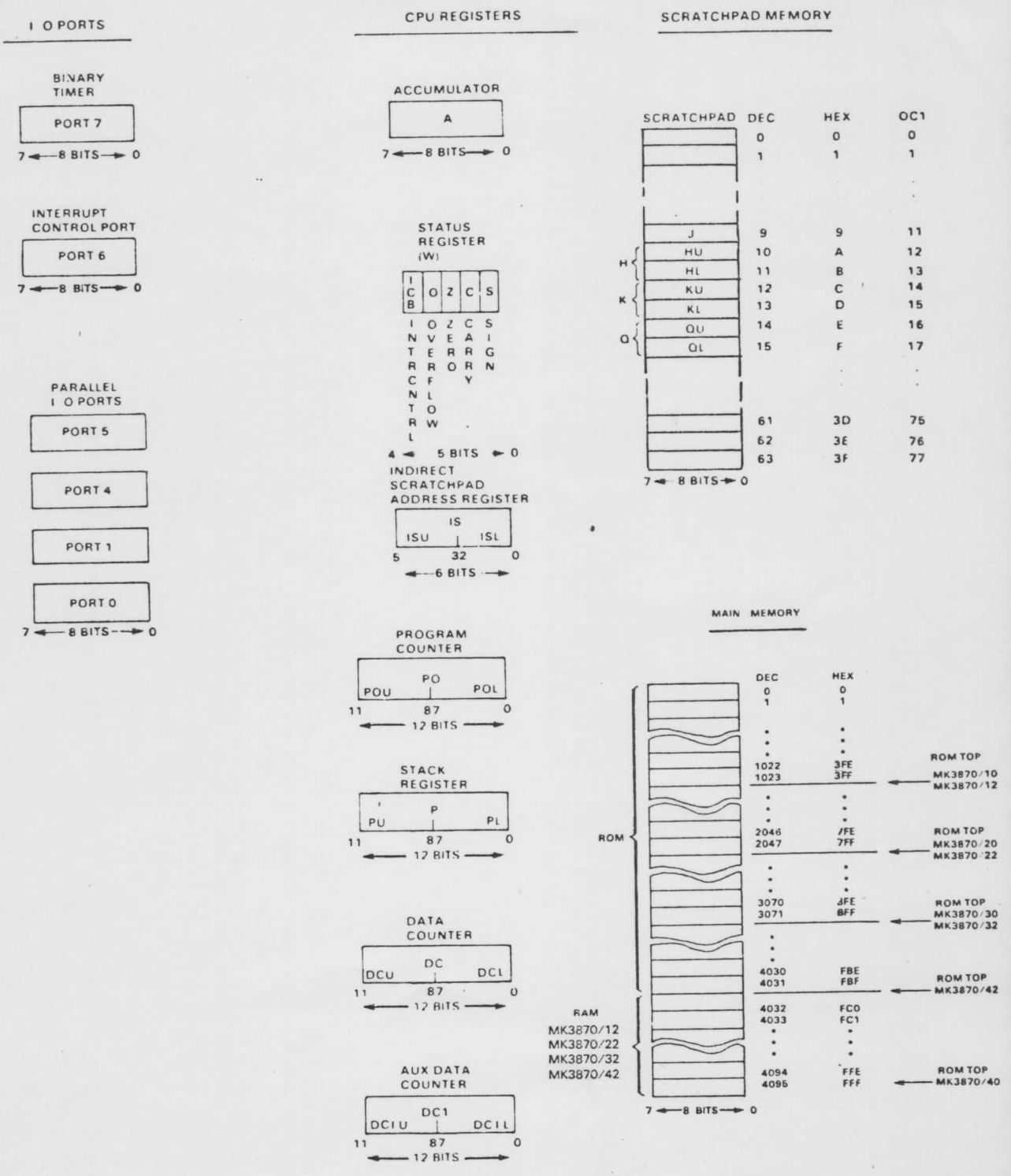
V_{CC} is the power supply input (single +5v).

MK3870 ARCHITECTURE

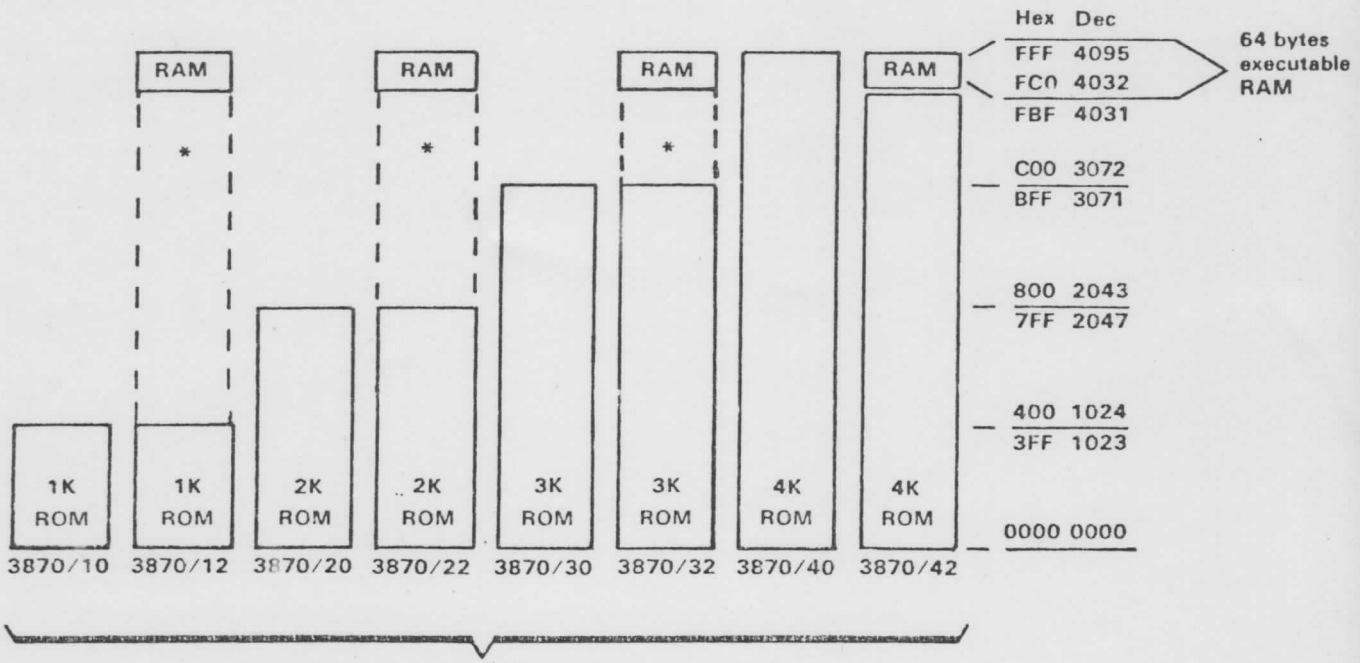
The basic functional elements of the MK3870 are shown in Figure 1. A programming model is shown in Figure 2. The architecture is common to all members of the 3870 family. All 3870 devices are instruction set compatible and differ only in amount and type of ROM, RAM, and I/O. The unique features of the MK3870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to all 3870 family devices.

MK3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3870 MAIN MEMORY
SIZES AND TYPES BY SLASH NUMBERS
Figure 3



All devices contain 64 bytes of scratchpad RAM.

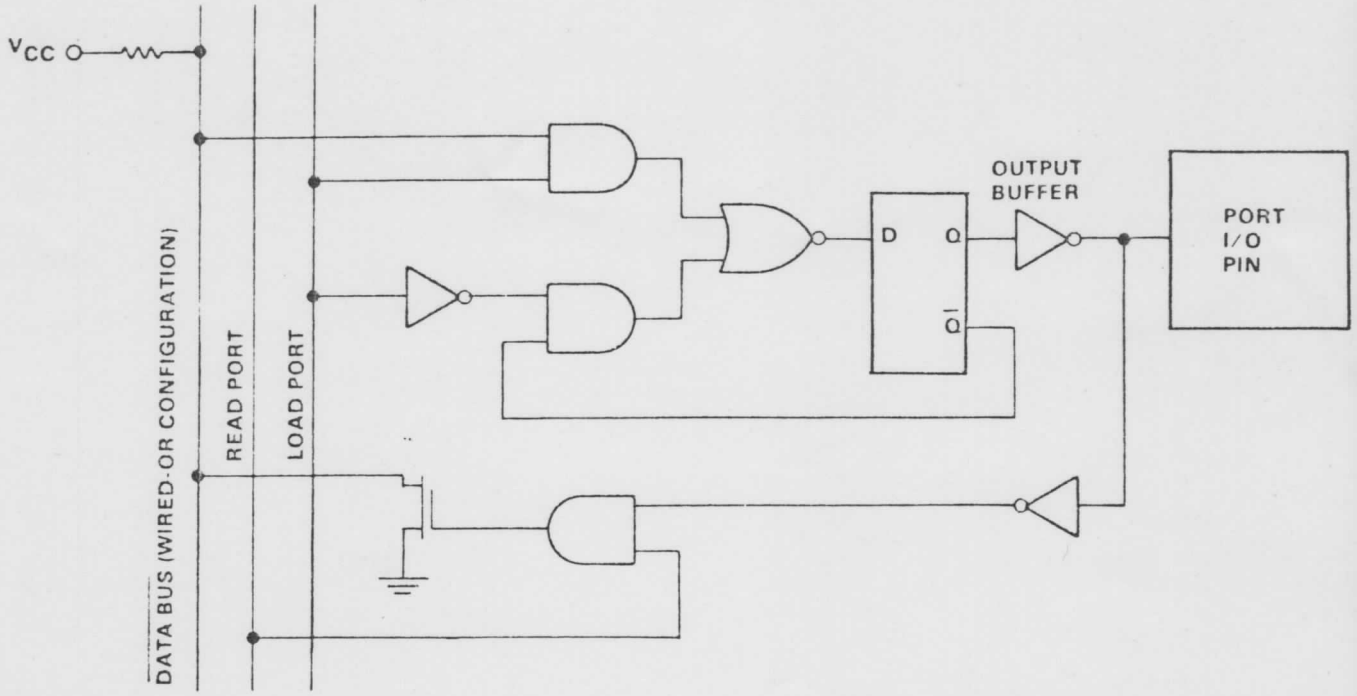
*Data derived from addressing these intermediate locations is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK3870/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3870/12	64 bytes	12 bits	1024 bytes	64 bytes
MK3870/20*	64 bytes	12 bits	2048 bytes	0 bytes
MK3870/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3870/30	64 bytes	12 bits	3072 bytes	0 bytes
MK3870/32	64 bytes	12 bits	3072 bytes	64 bytes
MK3870/40	64 bytes	12 bits	4096 bytes	0 bytes
MK3870/42	64 bytes	12 bits	4032 bytes	64 bytes

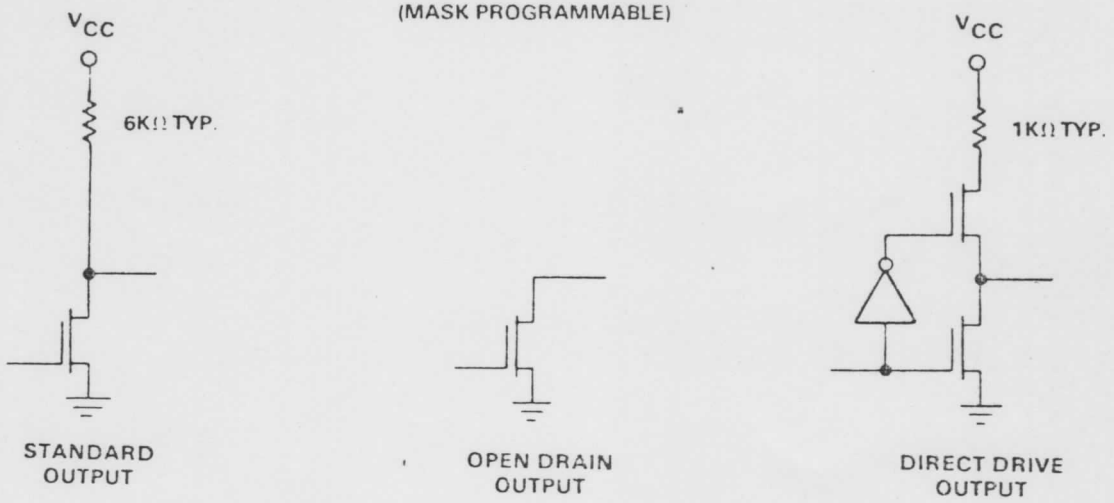
*The MK3870/20 is equivalent to the original 3870 device in memory size; however, the original 3870 had an 11-bit Address Register. The original 3870 with 11-bit Address Register is available where required. Consult the section describing ROM Code Ordering Information for additional information.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



OUTPUT BUFFER OPTIONS
(MASK PROGRAMMABLE)



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable).

MK3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 3 shows the amounts of ROM and executable RAM for every available slash number in the MK3870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK3870 devices is RAM memory. As with the ROM memory, the RAM may be addressed by the P0 and the DC address registers. The executable RAM may be addressed by all MK3870 instructions which address Main Memory. Additionally, the MK3870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

MK3870 CLOCKS

The time base network used with the MK3870 may be one of the four different types listed below.

Crystal
LC
RC
External Clock

The type of network which is to be used with the MK3870 is to be specified at the time when mask ROM MK3870 devices are ordered. The time base specifications for each of the four modes are covered in the 3870 Family Technical Manual.

MK38P70 GENERAL DESCRIPTION

The MK38P70 is the EPROM version of the MK3870. It retains an identical pinout with the MK3870, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P70 is housed in the "R" package which incorporates a 28-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P70 can act as an emulator for the purpose of exact verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P70 eliminates the need for emulator board products. In addition, several MK38P70s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3870s. The compact size of the MK38P70/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P70 can be used as the actual production device.

Most of the material which has been presented for the MK3870 in this document applies to the MK38P70. This includes the description of the pin configuration, architecture, programming model, and I/O ports. Additional information is presented in the following sections.

MK38P70 MAIN MEMORY

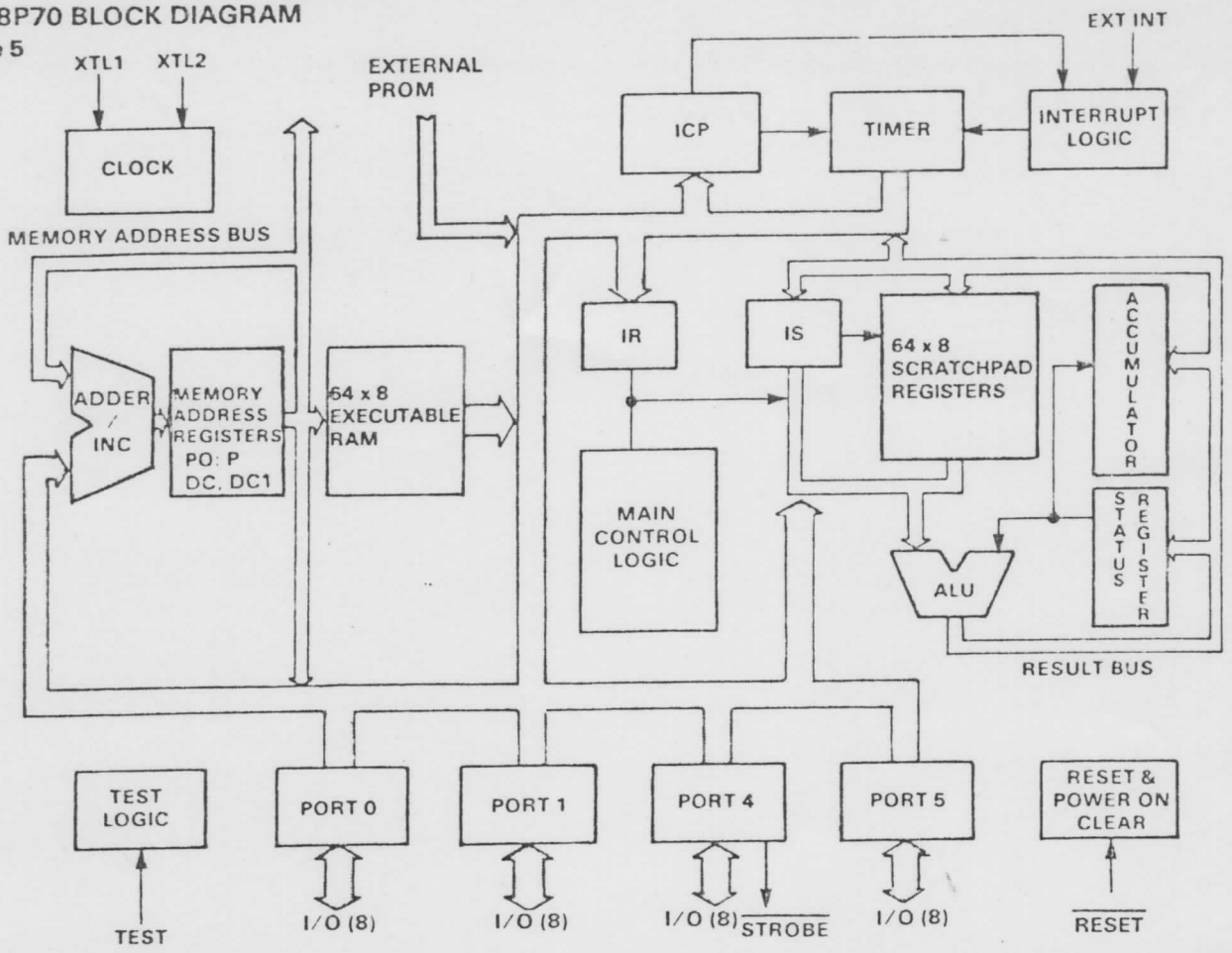
As can be seen from the block diagram in Figure 5, the MK38P70 contains executable RAM in the main memory map. The MK38P70 contains no on-chip ROM. Instead, the memory address lines are brought out to the 28 pin socket located directly on top of the 40 pin package, so the external EPROM memory is addressed as main memory.

There is one memory version of the MK38P70 and it is designated as the MK38P70/02. The MK38P70/02 contains 64 bytes of on-chip executable RAM. The MK38P70/02 can emulate the following devices.

MK3870/10
MK3870/12
MK3870/20
MK3870/22
MK3870/30
MK3870/32
MK3870/42

MK38P70 BLOCK DIAGRAM

Figure 5



The MK38P70/02 cannot exactly emulate the MK3870/40 because of the 64 bytes of executable RAM in the upper ROM space of the MK3870/40.

Addressing of main memory on the MK38P70 is accomplished in the same way as it is for the MK3870. See Figure 6 for main memory addresses and for address register size in the MK38P70.

MK38P70 EPROM SOCKET

A 28 pin EPROM socket is located on top of the MK38P70 "R" package. The socket and compatible EPROM memories are shown in Figure 7. When 24 pin memories are used in the 28 pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24 pin memory should be lower justified in the 28-pin socket).

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P70.

Initially, the MK38P70 that is compatible with the MK2716 is available. The MK38P70 designed to accomodate the 28-pin memory devices will be available at a later date.

MK38P70 I/O PORTS

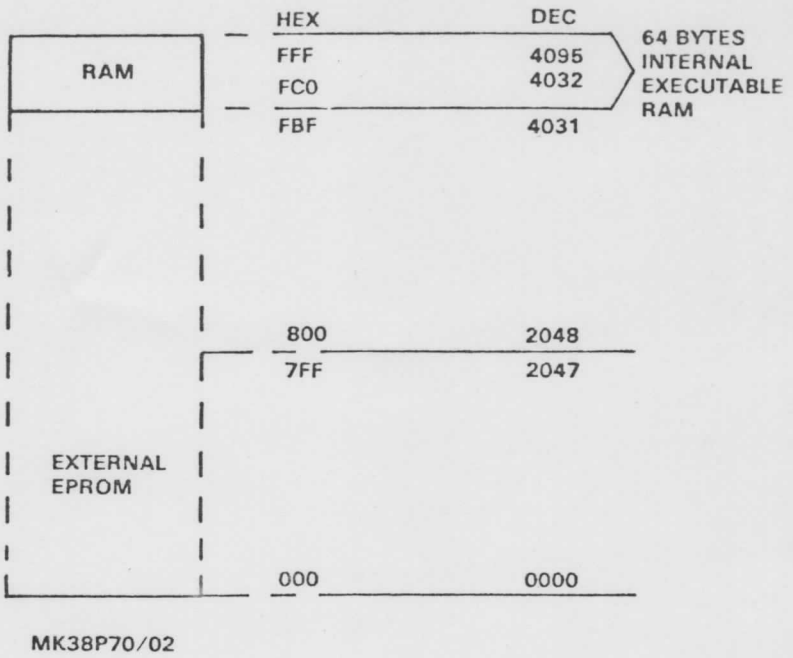
The MK38P70 is offered with two types of output buffer options on Ports 4 and 5. These are the open drain output buffer and the standard output buffer which are pictured in Figure 4. The open drain version of the MK38P70 is provided so that user-selected open drain port pins on the MK3870 can be emulated prior to ordering those mask ROM devices. Figure 7 lists which version(s) of the MK38P70 has open drain output buffers and which has standard output buffers in parentheses following the specified MK38P70 part ordering number (MK97XXX).

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P70 is shown in the next table. The Φ clock signal is derived internally in the MK38P70 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P70 which corresponds to a machine cycle, during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles, respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing

MK38P70 MAIN MEMORY MAP

Figure 6



MK38P70/02

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P70/02	64 bytes	12 bits	0 bytes	64 bytes

diagram. After a delay from the falling edge of the WRITE clock, the address lines become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P70 version is shown as t_{aas} or the time when address is stable until data must be valid on the data bus lines. The equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is shown in the following table.

MK38P70 CLOCKS

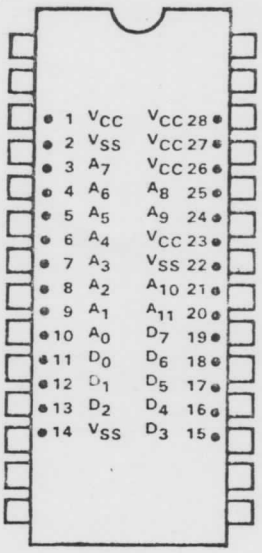
The MK38P70 has the ability to operate with any one of the following time base configurations.

Crystal
LC
RC
External Clock

This capability has been provided in the MK38P70 so that it can emulate a mask ROM MK3870 operating in any of the possible clock configurations.

MK38P70 "R" PACKAGE SOCKET PINOUT

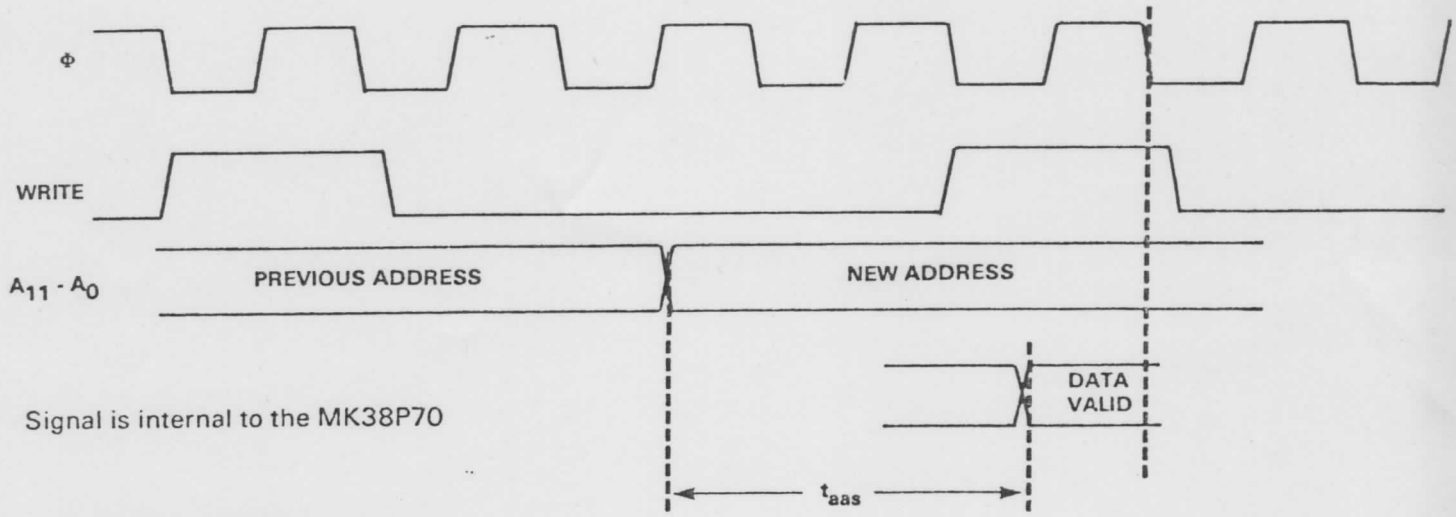
Figure 7



MK97400 (Standard Outputs) Compatible Memories	MK97410 (Open Drain) Compatible Memories
2758	2758
MK2716	MK2716
2516	2516
2532	2532

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P70

Figure 8



Signal is internal to the MK38P70

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850\text{ns}$$

(FROM ADDRESS STABLE)

	4MHz	3.58MHz	3MHz	2.5MHz	2MHz
ACCESS TIME	650ns	825ns	1.15μs	1.55μs	2.15μs

ELECTRICAL SPECIFICATIONS
MK3870, MK38P70

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temprature T_A
— 00	+5V ± 10%	0°C - 70°C
— 05	+5V ± 5%	0°C - 70°C
— 10	+5V ± 10%	-40°C - +85°C
— 15	+5V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_0	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load= 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time ·01		power supply rise time · 15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P70

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW. (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11} - A_0' stable until data must be valid at D_7-D_0	650				ns	Φ = 2.0 MHz

*See Table in Figure 8.

CAPACITANCE

T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance		10	pF	Unmeasured Pins Grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/10 Outputs Open
			94		125	mA	MK3870/12 Outputs Open
			85		110	mA	MK3870/20 Outputs Open
			94		125	mA	MK3870/22 Outputs Open
			100		130	mA	MK3870/30 Outputs Open
			100		130	mA	MK3870/32 Outputs Open
			100		130	mA	MK3870/40 Outputs Open
			100		130	mA	MK3870/42 Outputs Open

DC CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		125		150	mA	MK38P70/02 No EPROM, Outputs Open
P_D	Power Dissipation		400		525	mW	MK3870/10 Outputs Open
			440		575	mW	MK3870/12 Outputs Open
			400		525	mW	MK3870/20 Outputs Open
			440		575	mW	MK3870/22 Outputs Open
			475		620	mW	MK3870/30 Outputs Open
			475		620	mW	MK3870/32 Outputs Open
			475		620	mW	MK3870/40 Outputs Open
			475		620	mW	MK3870/42 Outputs Open
			600		750	mW	MK38P70/02 No EPROM, Outputs Open

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current pins with standard pull-up resistor	-100 -30		-89 -25		μA μA	$V_{OH}=2.4V$ $V_{OH}=3.9V$
I_{OHDD}	Output high current, direct drive pins	-100 -1.5 -8.5		-80 -1.3 -11		μA mA mA	$V_{OH}=2.4V$ $V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	$V_{OL}=2.4V$
I_{OL}	Output low current	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	$V_{OL}=0.4V$

DC CHARACTERISTICS FOR MK38P70

(Signals brought out at socket)

T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
I_{CCE}	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.8	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100		-90		μA	V_{OH}=2.4V
		-30		-25		μA	V_{OH}=3.9V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

1. $\overline{RESET}$ and EXT INT have internal Schmit triggers giving minimum .2V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(|I_{IL}|) = \Sigma (V_{CC} - V_{OH})(|I_{OH}|) = \Sigma (V_{OL})(I_{OL})$

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... + tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... -5tΦ to - (tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1) ..... + tΦ to - (tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... -5tΦ ± to - (tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... + tΦ to -(tpsc + 2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

Event Counter Mode:

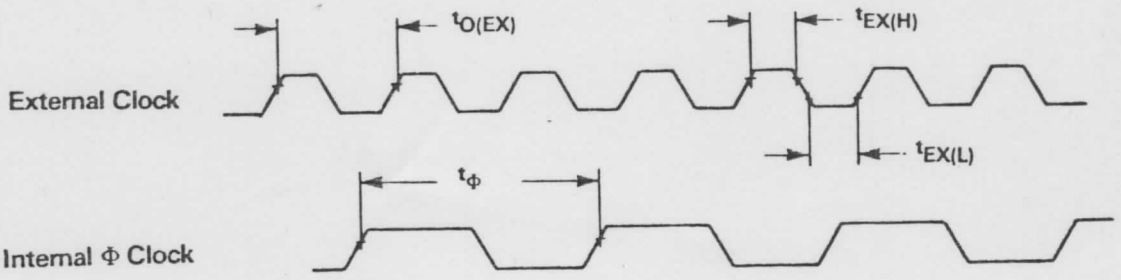
Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

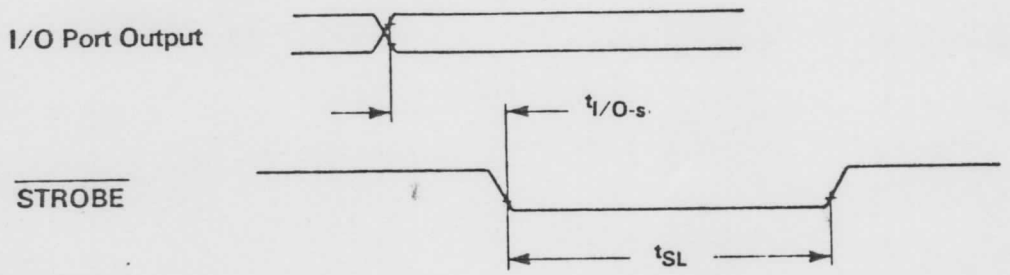
Notes:

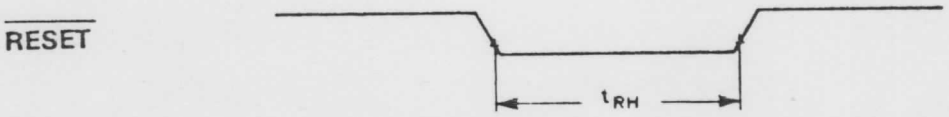
1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

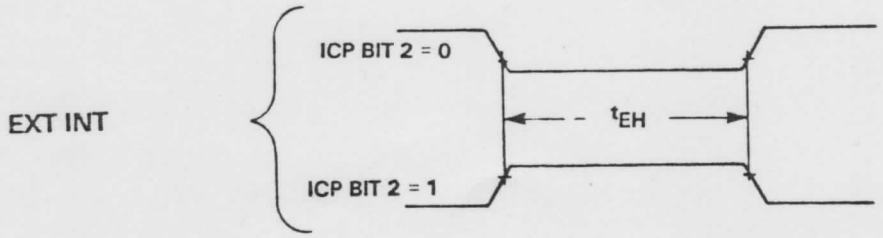
AC TIMING DIAGRAM

Figure 10





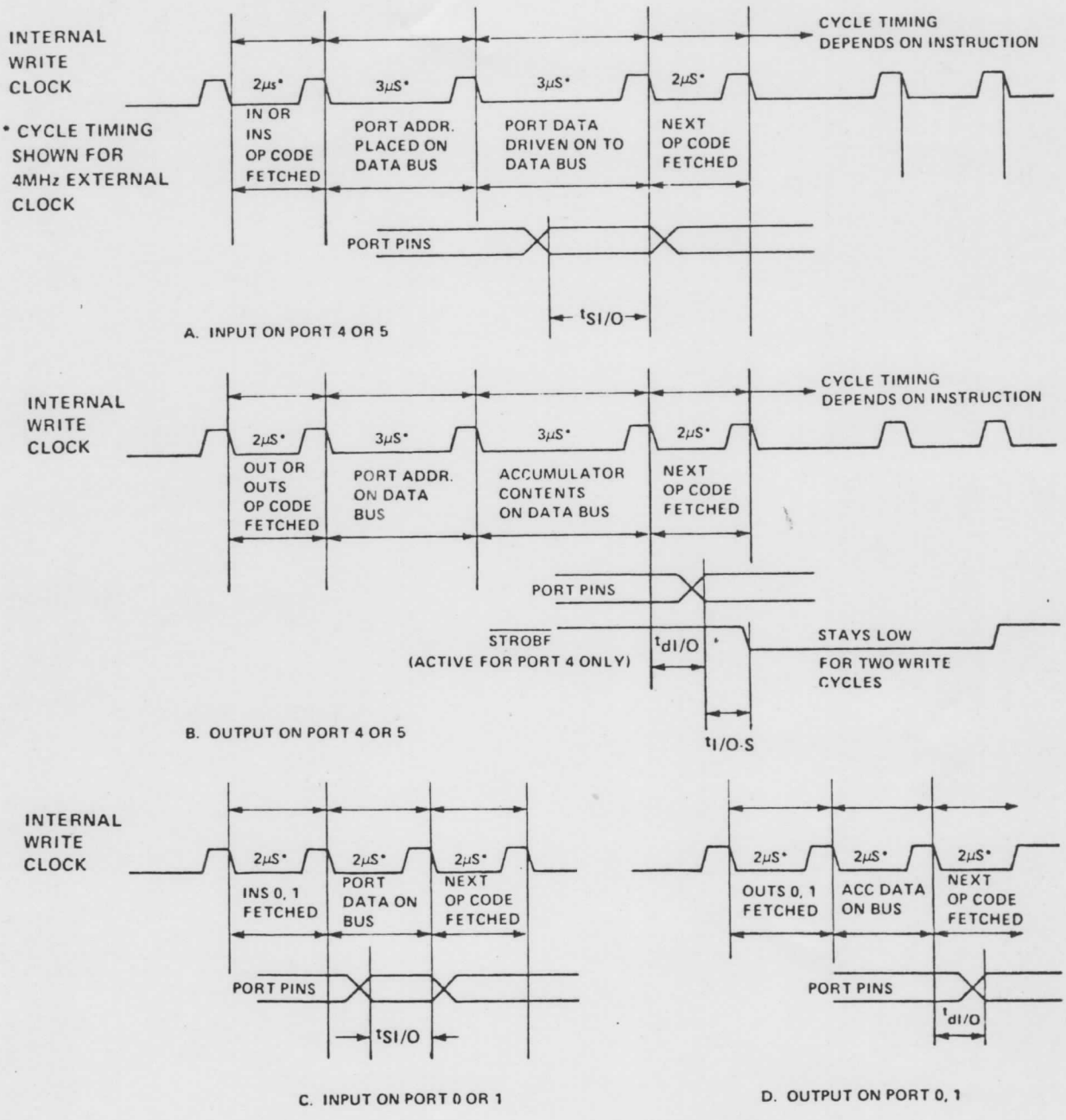




Note: All measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} max., or V_{OH} min.

INPUT/OUTPUT AC TIMING

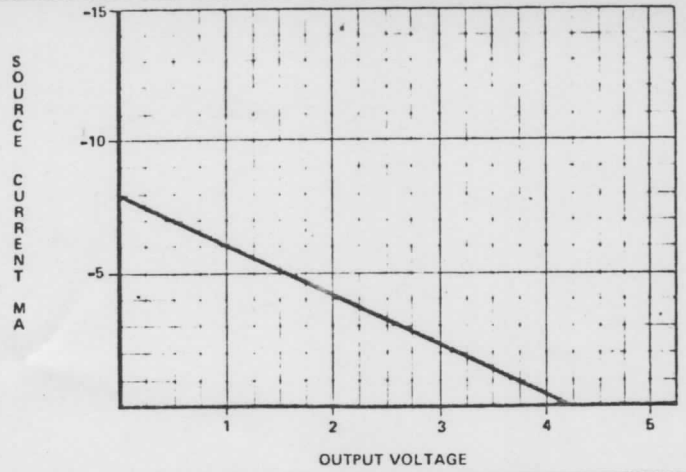
Figure 11



STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

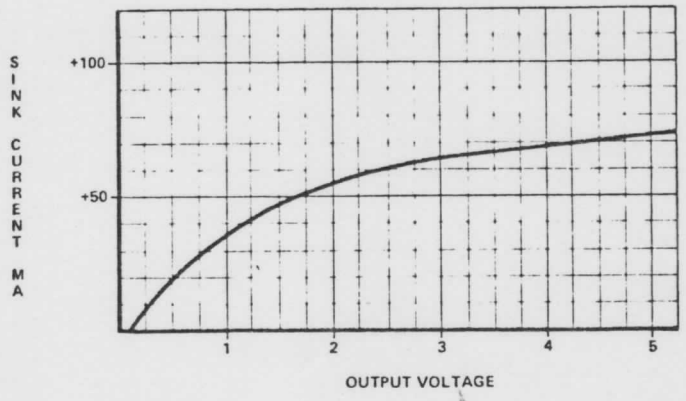
Figure 12



STROBE SINK CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

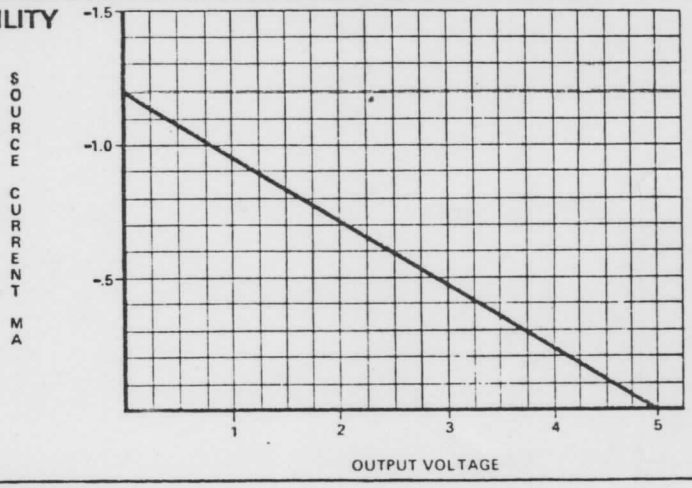
Figure 13



STANDARD I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

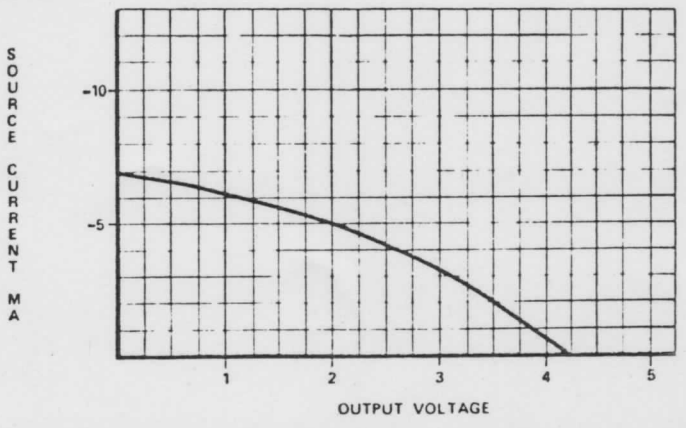
Figure 14



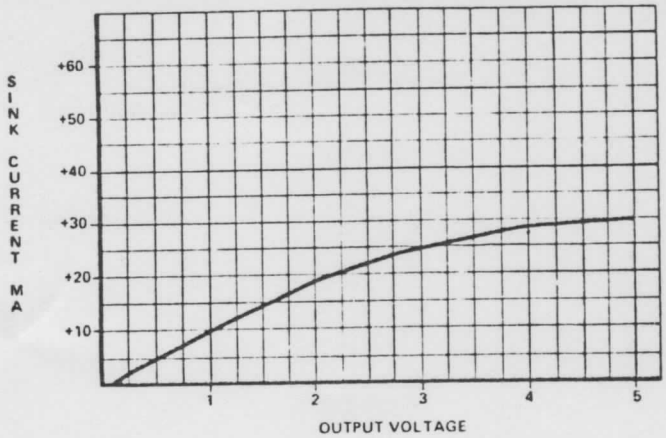
DIRECT DRIVE I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

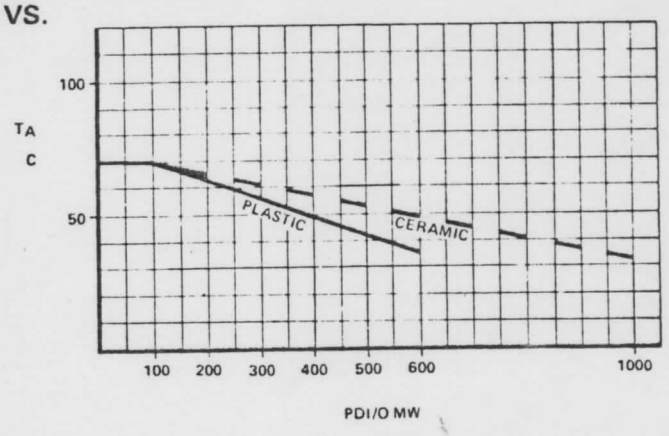
Figure 15



I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 16



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION
Figure 17

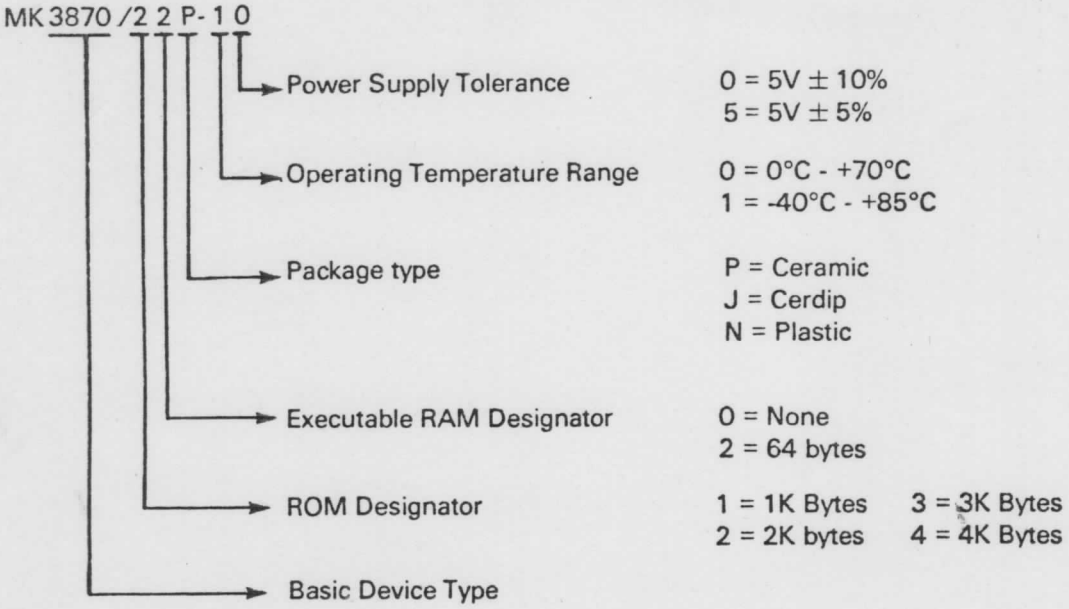


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number. Note: the specific device order number will be used to differentiate between the MK3870/20 with 12-bit Address Registers and the original 3870 with 11-bit Address Register, as mentioned in an earlier section.

GENERIC PART NUMBER

An example of the generic part number is shown below.

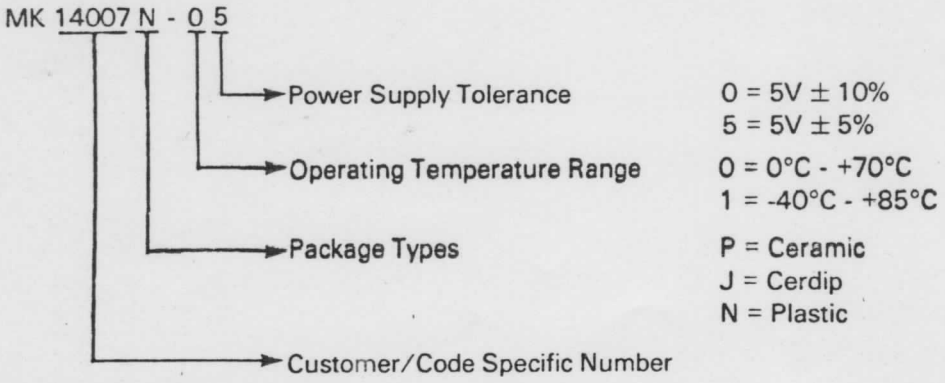


An example of the generic part number for the EPROM device is shown below.

MK38P70/02 R-05

DEVICE ORDER NUMBER

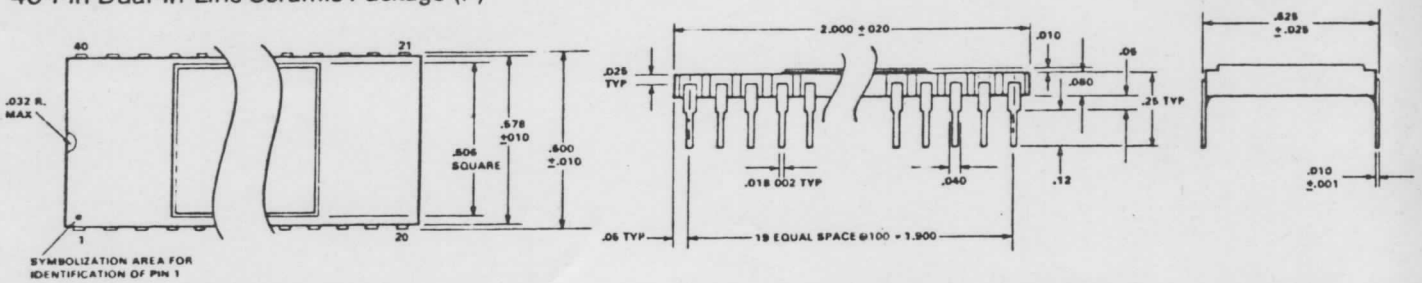
An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

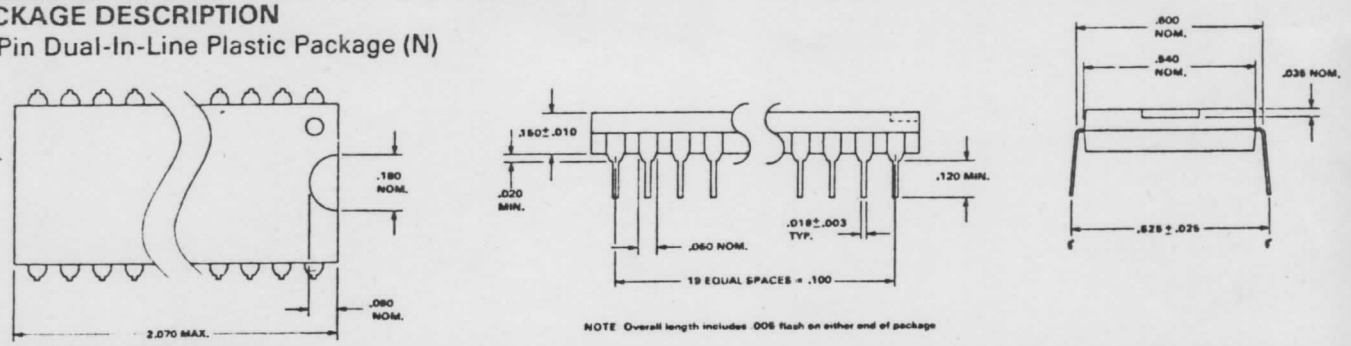
PACKAGE DESCRIPTION

40-Pin Dual-In-Line Ceramic Package (P)



PACKAGE DESCRIPTION

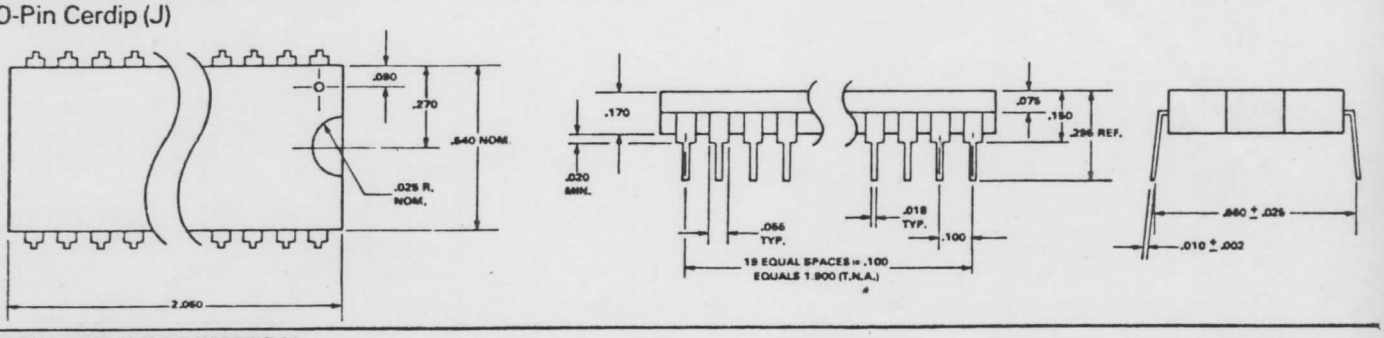
40-Pin Dual-In-Line Plastic Package (N)



NOTE Overall length includes .005 flash on either end of package

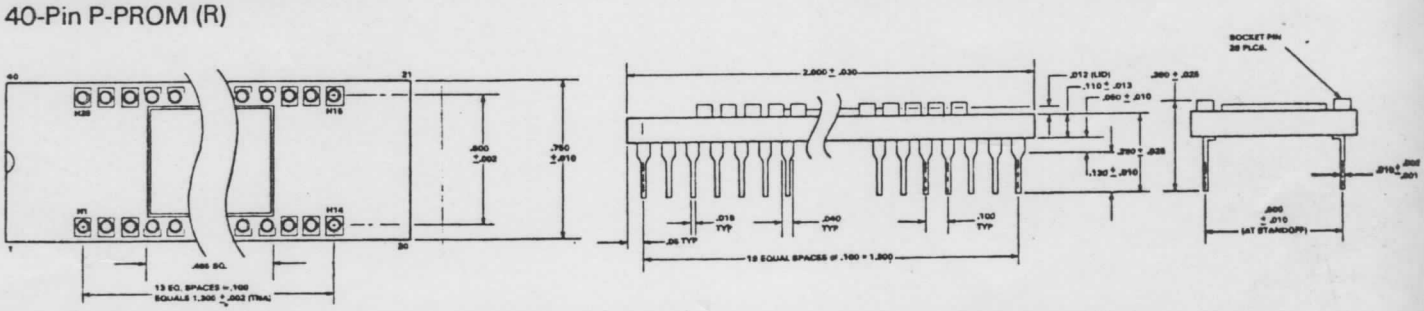
PACKAGE DESCRIPTION

40-Pin Cerdip (J)



PACKAGE DESCRIPTION

40-Pin P-PROM (R)



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